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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/585,914	07/13/2006	Satoshi Miura	0524-0163	1642

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COOK ALEX LTD
SUITE 2850
200 WEST ADAMS STREET
CHICAGO, IL 60606

EXAMINER	
TRAN, ANH Q	
ART UNIT	PAPER NUMBER
2819	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/585,914	MIURA ET AL.	
	Examiner	Art Unit	
	ANH Q. TRAN	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 9-14* is/are rejected.

7)☒ Claim(s) *5-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 July 2006* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/15/08, 1/26/07, 7/13/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 10 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite in that it fails to point out what is included or excluded by the claim language. This claim is an omnibus type claim.

Claim Objections

3. Claim 10 is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claims 9 and 2. See MPEP § 608.01(n). Accordingly, the claim has not been further treated on the merits.

4. Claim 12 is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claims 11 and 2. See MPEP § 608.01(n). Accordingly, the claim has not been further treated on the merits.

5. Claim 11 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. An NMOS transistor connected to the power supply potential on the high potential side and a PMOS transistor connected to the power supply potential on the low potential side did not further limit the subject matter of a previous claim but replaced the subject matter of the previous claim.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 13-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Oner et al. (7,012,450).

Claim 1, Oner shows a differential drive circuit for low voltage differential signals (Fig. 4), comprising:

a switching circuit composed of MOS transistors (102, Fig. 4), and configured to be inputted thereto with differential signals (D and DB) and to output current signals (A and B);

an output circuit including an NMOS transistor (2) connected at its one end to a power supply potential on a high potential side (VDD) and at its other end to one node (N5) in the switching circuit, and operating as a source follower; and

a PMOS transistor (12) connected at its one end to a power supply potential on a low potential side (ground) and at its other end to other node (N10) in the switching circuit and operating as a source follower; and

a reference potential generating circuit (200, 20, 22) that supplies reference potentials to gates of the NMOS transistor (output from 20) and the PMOS transistor

(output from 22), respectively, wherein the reference potential generating circuit includes potential variable means (200) for changing a differential potential with an offset potential being kept constant.

Claim 2, Oner shows the differential drive circuit for low voltage differential signals according to claim 1, wherein the switching circuit includes:

a first transistor (4) and a second transistor (6) connected at their one ends to a source of the NMOS transistor, forming a node; and

a third transistor (8) and a fourth transistor (10) connected at their one ends to a source of the PMOS transistor, forming a node, a node (A) at which the first transistor and the third transistor are connected at their other ends and a node (B) at which the second transistor and the fourth transistor are connected at their other ends form output terminals of the output circuit, and

a node (D) at which the first transistor and the fourth transistor are connected at their gates and a node (DB) at which the second transistor and the third transistor are connected at their gates form input terminals for the differential signals.

Claim 13, Bu shows an electronic apparatus comprising a differential drive circuit for low voltage differential signals according to any one of claims 1 through 12.

Claim 14, Bu shows the electronic apparatus according to claim 13, wherein the electronic apparatus is constituted by a mobile terminal (the LVDS is for telecommunication system which are inherently in the mobile terminal).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oner et al. (7,012,450) in view of Tomita (6,292,028).

Claim 3, Oner discloses the claimed device except for the reference potential generating circuit includes: a first resistor connected between the power supply potential on the high potential side and the gate of the NMOS transistor; a second resistor connected between the gate of the NMOS transistor and the gate of the PMOS transistor; and a third resistor connected between the gate of the PMOS transistor and the power supply potential on the low potential side.

Tomita discloses the reference potential generating circuit (Fig. 16) includes: a first resistor (R1301) connected between the power supply potential (Vdd) on the high potential side and a gate of a MOS transistor; a second resistor (R1302) connected between the gate of the MOS transistor and a gate of another MOS transistor; and a third resistor (R1303) connected between the gate of the another MOS transistor and the power supply potential on the low potential side (ground).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the reference potential generating circuit of Tomita in

place of the reference potential circuit (200, Fig. 4) of Oner, as taught by Tomita in order to has an advantage of an exceedingly simple circuit configuration.

Claim 4, Oner in view of Tomita discloses the claimed invention except for the first resistor and the third resistor in the reference potential generating circuit have an equal resistance value. It would have been an obvious matter of design choice to provide the first resistor and the third resistor in the reference potential generating circuit have an equal resistance value, since such a modification would have involved a mere change in the size of a component for equal resistance value. A change in size is generally recognized a being within the level of ordinary skill in the art.

5. Claims 1, 9, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Radelinow (6,977,534) in view of Li (6,867,618).

Claim 1, Radelinow shows a differential drive circuit for low voltage differential signals (Fig. 3), comprising:

a switching circuit composed of MOS transistors (MP5, MP6, MN5, MN6), and configured to be inputted thereto with differential signals (A and A_bar) and to output current signals (OUT1 and OUT2);

an output circuit including an PMOS transistor (MP3) connected at its one end to a power supply potential on a high potential side and at its other end to one node in the switching circuit, and operating as a source follower; and

a NMOS transistor connected at its one end to a power supply potential on a low potential side (ground) and at its other end to other node in the switching circuit and operating as a source follower; and

a reference potential generating circuit (MP1B-MP3B, MN1B-MN6B, SW1-SW3) that supplies reference potentials to gates of the NMOS transistor and the PMOS transistor, respectively, wherein the reference potential generating circuit includes potential variable means (RB1-RB3 and SW1-SW5) for changing a differential potential with an offset potential being kept constant.

Radelinow discloses the claimed invention except for an NMOS transistor and connected at its one end to a power supply potential on a high potential side and at its other end to one node in the switching circuit, and operating as a source follower; and

a PMOS transistor connected at its one end to a power supply potential on a low potential side (ground) and at its other end to other node in the switching circuit and operating as a source follower.

However, Li teaches that it is known to implement an NMOS transistor (300, Fig. 4) and connected at its one end to a power supply potential (VDD) on a high potential side and at its other end to one node (Vhigh) in the switching circuit (110a-121a), and operating as a source follower; and

a PMOS transistor (301) connected at its one end to a power supply potential on a low potential side (ground) and at its other end to other node (Vlow) in the switching circuit and operating as a source follower as set forth at column 5, lines 47-65).

It would have been obvious to one having ordinary skill in the art at the time the time the invention was made to replace the PMOS transistor connected at its one end to a power supply potential on a high potential side with the NMOS transistor; and

the NMOS transistor connected at its one end to a power supply potential on a low potential side (ground) with the PMOS transistor, as taught by Li in order to provide significantly lower impedance looking into the source follower, therefore, allows for better high-speed switching output from the different driver.

Claim 9, Radelinow shows the differential drive circuit for low voltage differential signals according to claim 1,

wherein output terminals of the output circuit are connected to output terminals of an emphasis circuit (Secondary stage),

wherein the emphasis circuit includes a switching circuit for the emphasis circuit constituted by MOS transistors (MP8, MP9, MN8, MN9), which are inputted thereto with different differential signals (B and B_bar), and output current signals (OUT1 and OUT2), one node in the switching circuit for the emphasis circuit being connected to a drain of a PMOS transistor (MP7), a source of the PMOS transistor connected to the power supply potential (VDD) on the high potential side, and a gate of the PMOS transistor connected to one terminal (MP1B transistor gate) of a bias power supply for the emphasis circuit, and wherein the other node in the switching circuit for the emphasis circuit is connected to a drain of an NMOS transistor (MN7), a source of the NMOS transistor being connected to the power supply potential on the low potential

side (ground), and a gate of the NMOS transistor being connected to the other terminal (MN6B transistor gate) of the bias power supply for the emphasis circuit.

Claim 11, Radelinow discloses the claimed invention except for the emphasis circuit is configured in such a manner that: one node in the switching circuit for the emphasis circuit is connected to a source of an NMOS transistor, a drain of the NMOS transistor is connected to the power supply potential on the high potential side, and a gate of the NMOS transistor is connected to one terminal of a bias power supply for the emphasis circuit; and the other node in the switching circuit for the emphasis circuit is connected to a source of a PMOS transistor, a drain of the PMOS transistor is connected to the power supply potential on the low potential side, and a gate of the PMOS transistor is connected to other terminal of the bias power supply for the emphasis circuit.

However, Li teaches that it is known to implement an NMOS transistor (300, Fig. 4) and connected at its one end to a power supply potential (VDD) on a high potential side and at its other end to one node (Vhigh) in the switching circuit (110a-121a), and operating as a source follower; and

a PMOS transistor (301) connected at its one end to a power supply potential on a low potential side (ground) and at its other end to other node (Vlow) in the switching circuit and operating as a source follower as set forth at column 5, lines 47-65).

It would have been obvious to one having ordinary skill in the art at the time the time the invention was made to replace the PMOS transistor (MP7, Fig. 4 of Radelinow)

connected at its one end to a power supply potential on a high potential side with the NMOS transistor; and

the NMOS transistor (MN7, Fig. 4 of Radelinow) connected at its one end to a power supply potential on a low potential side (ground) with the PMOS transistor, as taught by Li in order to provide significantly lower impedance looking into the source follower, therefore, allows for better high-speed switching output from the different driver.

Allowable Subject Matter

6. Claims 5-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANH Q. TRAN whose telephone number is (571)272-1813. The examiner can normally be reached on M-Th (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Anh Q. Tran/
Primary Examiner, Art Unit 2819
9/4/08